DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under

37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al.(US 6,257,760) in view of Akiyama et al.(US 6,245,647) and further in view of Yoon et al.(US 2003/0077870) if necessary.

Re. claim 1, Davis et al. teaches a process flow diagram in which a plurality of substantially similar superlattice structures are first formed by depositing alternating layers of distinctly different sub lattices upon silicon-based substrates. Thereafter, a resistivity versus temperature calibration curve is formed for the superlattice structures. To obtain the data required for the calibration curve, each of the superlattice structures is annealed in a furnace or a RTA unit at a different temperature for a pre-defined period of time. The range of anneal temperatures may vary, depending upon the temperature range of the fabrication process whose temperature is to be determined in subsequent steps. After a superlattice structure is annealed, it is desirable to allow the structure to cool down to at least room temperature. In this manner, interdiffusion of atoms between the sublattices of the superlattice structure is terminated. As such, the atoms within the superlattice structure are "frozen" at the positions they migrated to during the anneal process. The resistivity of each of the superlattice structures may then be measured in order to create the calibration curve(Figure 3, Abstract and Column 6,lines 56-67 and

Column 7,lines 1-9)(same as measuring a resistivity of arbitrary semiconductor substrates at a room temperature; obtaining respectively a relation between a heating temperature and a temperature of a surface of the arbitrary semiconductor substrates , for the arbitrary semiconductor substrates having different resistivities; setting and adjusting said heating temperature of a semiconductor substrate to be used based (i)a measured resistivity of the semiconductor substrate to be used and (ii) the obtained relationship between the heating temperature and the temperature of the surface of said semiconductor substrate)(The silicon substrate and similar superlattice structures are considered to be the semiconductor substrates) and then another superlattice structure (same as epitaxial layer) is grown , wherein the temperature of said surface of said semiconductor substrate to be used is indirectly controlled by adjusting said heating temperature(Column 7,lines 11-16) but does not teach a vapor phase growth method for growing an epitaxial layer on a substrate.

However, Akiyama et al. teaches a method for forming a thin film uniform in resistivity distribution on a semiconductor substrate. The temperature of the inside wall (6) of the reaction vessel (2) of vapor phase growth equipment is controlled to below the thermal decomposition temperature of a dopant gas such as diborane (abstract) and vapor phase epitaxial growth of a silicon semiconductor single crystal thin film was conducted under the following conditions(Column 6,lines 61-68)(same as growing the epitaxial layer, wherein the temperature of said surface of said semiconductor substrate to be

used is indirectly controlled by adjusting said heating temperature) to form a thin film uniform in resistivity distribution on a semiconductor substrate.

Therefore it would have been obvious for one with ordinary skill in the art at the time the invention was made to provide Davis et al. structure with growing the epitaxial layer, wherein the temperature of said surface of said semiconductor substrate to be used is indirectly controlled by adjusting said heating temperature of Akiyama et al. to form a thin film uniform in resistivity distribution on a semiconductor substrate.

Re. claim 2 as discussed above in claim 1 , Davis et al. and Yoon et al. and Akiyama et al. in combination disclose all the limitations as discussed above in claim 1 including wherein the semiconductor substrate is a compound semiconductor(i.e. Fe-doped InP substrate)(Para[0016], Yoon et al.).

Re. claim 3 as discussed above in claim 2, Davis et al. and Yoon et al. and Akiyama et al. in combination disclose all the limitations as discussed above in claim 2 including wherein the semiconductor substrate is an InP substrate(Para[0016], Yoon et al.).

Re. claim 4 as discussed above in claim 3, Davis et al. and Yoon et al. and Akiyama et al. in combination disclose all the limitations as discussed above in claim 3 including

wherein the semiconductor substrate is an Fe-doped In P substrate(Para[0016], Yoon et al.).

Re. claim 5 as discussed above in claims 1 to 4 , Davis et al. and Yoon et al. and Akiyama et al. in combination disclose all the limitations as discussed above in claims 1 to 4 including wherein a molecular beam epitaxy is used to grow an epitaxial layer(Para[0016], Yoon et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANKUSH k. SINGAL whose telephone number is (571)270-1204. The examiner can normally be reached on monday-friday 7am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2895

/A. k. S./
Examiner, Art Unit 2895